TAJIRI, M.
Serial No. 10/700,467

Atty Dkt: 4074-10
Art Unit: 2827

AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 13, and continuing to page 1, line 23, as follows:

Among nonvolatile memories ~~on which researches are currently conducted~~undergoing current research, great attention is ~~focussed~~ focused on a memory device using nonvolatile variable resistors in each of which a difference in resistance value (hereinafter, simply referred to as "resistance" in some cases) is read in a current as in MRAM (Magneto-resistive Random Access Memory) or OUM (Ovonic Universal Memory) because of its high write durability and high speed operation. This memory has an advantage that no dimensional limit in accordance with statistical physics exists in microfabrication, which DRAM, flash memory and FeRAM (Ferroelectric Random Access Memory) suffer.

Please amend the paragraph beginning at page 1, line 24, and continuing to page 2, line 22, as follows:

Fig. 7 is a descriptive view showing an outline of a memory device using a conventional nonvolatile variable resistor. Such a nonvolatile variable resistor Rv is disclosed, for example, in U.S. Patent No. 6,204,139, B1. A reference numerical 1 indicates a first electrode, a nonvolatile variable resistance body 2 is formed in the form of a film on the first electrode 1 and a second electrode 3 is formed on the nonvolatile variable resistance body 2, thereby constituting the nonvolatile variable resistor Rv. The nonvolatile variable resistor Rv is formed on a surface of a substrate 9 with an insulating property. By applying a pulse power supply Vp between the first electrode 1 and the second electrode 3 of the nonvolatile variable resistor Rv with such a structure, the nonvolatile variable resistor Rv works as a memory element (a memory device) operable

even at ordinary temperature. Examples of the nonvolatile variable resistance body 2 that have been known include a manganese oxide of a perovskite structure, such as $Pr_{0.7}Ca_{0.3}MnO_3$~~Pr.sub.0.7Ca.sub.0.3MnO.sub.3~~. While a resistance value of the nonvolatile variable resistance body 2 is changed by a pulse voltage applied thereto, the nonvolatile variable resistance body 2 has a nonvolatility to sustain the resistance value thereof even when power supply is turned off. Arrangement of a large number of nonvolatile variable devices Rv in a matrix enables a memory device to be formed on the substrate 9.

Please amend the paragraph beginning at page 2, line 23, and continuing to page 3, line 13, as follows:

Fig. 8 is a graph showing a way of ~~a change in~~changing a resistance value with respect to application of a voltage pulse in the memory device of Fig. 7. The abscissa represents the number of applied pulses (applied pulse code) and the ordinate represents a resistance value (Ω) ~~wherein~~. In Fig. 7, a voltage of an applied pulse is 2.9 V, a pulse width is 17 ns, and a pulse polarity is positive (+) or negative (–). For example, a first pulse (applied pulse code 1) is negative and a resistance value after application of the first pulse changes (increases) from 10^4 to 10^6. A second pulse (applied pulse code 2) is positive, and a resistance value after application of the second pulse changes (decreases) from 10^6 to 10^4. This difference (change) in resistance can be stored as a logical signal in correspondence to a logical value 1 or 0. Since the resistance value can be sustained when a power supply is turned off, the memory device can be used as nonvolatile.

Please amend the paragraph beginning at page 4, line 23, and continuing to page 5, line 10, as follows:

~~Herein, a definition will be done such that, for example,~~As used herein, an operation for raising a resistance is a "write" and an operation for reducing a resistance is "reset" ~~(the definition being hereinafter adopted in the description to come)~~. In a write operation, a positive voltage pulse is applied onto the bit line BL, while the source line SL is driven to a ground potential. In "reset", the bit line BL is driven to the ground potential, while a positive voltage pulse is applied onto the source line SL. That is, since ~~in write and rest,~~ opposite pulses (pulses of different polarities, positive and negative) are respectively applied ~~on~~to the nonvolatile variable resistance body 2 during the write and reset operations, ~~a~~ resistance can be changed.

Please amend the paragraph beginning at page 5, line 11, and continuing to page 5, line 19, as follows:

~~As one of other rewrite methods in a 1T1R type memory cell, t~~The following method has also been available as another rewrite methods in a 1T1R type memory cell. In this method, in write, similar to the write described above, a positive voltage pulse is applied onto the bit line BL, while the source line SL is driven to ~~the~~ ground potential. In reset, the bit line BL is driven to ~~the~~ ground potential, while a voltage (an amplitude) of a positive voltage pulse applied onto the source line SL is rendered smaller and a pulse width thereof is rendered longer than in the write.

Please amend the paragraph beginning at page 5, line 25, and continuing to page 6, line 11, as follows:

In a case where rewrite is conducted in a 1D1R type memory cell, a potential on the word line WL of a selective cell is at first raised, while the bit line BL is driven to a ground potential. At this time, in memory cells other than the selective cell (the memory cells being hereinafter referred to as non-selective cells), word lines WL are driven to ~~the~~ ground potential while potentials on bit lines BL are set to a positive potential to thereby cause the diodes 6 to take ~~an~~ rectifying action, therefore applying no voltage to the non-selective cells. A voltage (an amplitude) of a voltage pulse in reset renders a voltage of a voltage pulse in write to be smaller, and a pulse width is rendered longer than in write.

Please amend the paragraph beginning at page 8, line 23, and continuing to page 9, line 10, as follows:

~~Since a l~~Larger capacity ~~is~~ has also been requested ~~in a~~ for memory devices using ~~the~~ nonvolatile variable resistors Rv ~~as well,~~. Accordingly, investigations have attempted ~~it has been studied~~ to reduce a projected area on a plane of a memory cell (especially, a projected area on a plane of the nonvolatile variable resistance body) by means of scaling. ~~Since in the structure of a conventional nonvolatile variable resistor, h~~However, if a projected area on a plane of the nonvolatile variable resistance body (the first electrode and the second electrode) of a conventional nonvolatile variable resistor is reduced by means of scaling, ~~a~~ resistance increases in inverse proportion to the reduction ratio of the projected area~~, there has been~~. This leads to a problem ~~that as~~ described below: a time constant ($\tau = CR$) in a memory cell increases ~~to~~ and thereby slows ~~an~~ operation.

Please amend the paragraph beginning at page 11, line 18, and continuing to page 12, line 9, as follows:

In Fig. 14B, the abscissa represents time (μs) while the ordinate represents a relative potential with a saturated value of a potential on a bit line BL being set to 100. A time constant τ of a curve T1 is 10 μs, a time constant τ of a curve T2 is 1 μs, a time constant τ of a curve T3 is 100 ns and a time constant τ of a curve T4 is 10 ns. For example, in a case where, in the curve T3, a resistance of 100 is increased 25 times (that is to resistance of 2500), a time constant τ (= CR) increases from 100 ns to 2500 ns (2.5 μs) in accordance with a simple calculation. That is, a change in potential on a bit line BL, which was on the curve T3, is slowed to a change in potential on a curve slower than on the curve T2, resulting in reduction in operating speed of a memory cell. In such a way, a problem has occurred that in a conventional nonvolatile variable resistor Rv, an operating speed, especially a read speed, is decreased in ~~company~~ accordance with an increase in resistance by scaling.

Please amend the caption at page 12, line 11,as follows:

BRIEF SUMMARY ~~OF THE INVENTION~~

Please amend the paragraphs beginning at page 13, line 5, and continuing to page 17, line 6, as follows:

~~According to the invention, a~~A nonvolatile variable resistor includes: a first electrode and a second electrode facing each other and formed on a substrate; and a nonvolatile variable resistance body formed between the first electrode and the second electrode, wherein the first electrode and the second electrode face each other in a direction of a surface of the substrate.

In a nonvolatile variable resistor according to ~~the inventionan~~ example embodiment, the nonvolatile variable resistance body is formed on an outer surface of the first electrode, and the second electrode is formed on an outer surface of the nonvolatile variable resistance body.

In a nonvolatile variable resistor according to ~~the inventionan~~ example embodiment, the first electrode is columnar or prismatic.

In a nonvolatile variable resistor according to an example embodiment~~the invention~~, the nonvolatile variable resistance body is made of a manganese oxide of a perovskite structure.

In a nonvolatile variable resistor according to an example embodiment~~the invention~~, the manganese oxide is any of

$Pr_{(1-x)}Ca_xMnO_3$~~Pr.sub.(1-x)Ca.sub.xMnO.sub.3~~,

$La_{(1-x)}Ca_xMnO_3$~~La.sub.(1-x)Ca.sub.xMnO.sub.3~~ and

$La_{(1-x-y)}Ca_xPb_yMnO_3$~~La.sub.(1-x-y)Ca.sub.xPb.sub.yMnO.sub.3~~.

In a nonvolatile variable resistor according to an example embodiment~~the invention~~, the manganese oxide is any of

$Pr_{0.7}Ca_{0.3}MnO_3$~~Pr.sub.0.7Ca.sub.0.3MnO.sub.3~~,

$La_{0.65}Ca_{0.35}MnO_3$~~La.sub.0.65Ca.sub.0.35MnO.sub.3~~ and

$La_{0.65}Ca_{0.175}Pb_{0.175}MnO_3$~~La.sub.0.65Ca.sub.0.175Pb.sub.0.175MnO.sub.3~~.

According to an example embodiment~~the invention~~, a memory device has arrangement of memory cells in a matrix on a substrate, each memory device being constituted of a nonvolatile variable resistor and a selective device, connected to the nonvolatile variable resistor, for selecting the nonvolatile variable resistor.

In a memory device according to an example embodiment~~the invention~~, the selective device selects one from the nonvolatile variable resistors to control a current applied to the one of the nonvolatile variable resistors.

In a memory device according to an example embodiment~~the invention~~, the selective device is a transistor or a diode formed on the substrate.

In a memory device according to an example embodiment~~the invention~~, the transistor is a MOS transistor, and a drain of the MOS transistor is connected to the first electrode.

In a memory device according to an example embodiment~~the invention~~, a cathode of the diode is connected to the first electrode.

In a memory device according to an example embodiment~~the invention~~, the memory cells each have a word line connected to the selective device and a bit line connected to the nonvolatile variable resistor, and the second electrode is connected to the bit line.

According to an example embodiment~~the invention~~, a scaling method of a nonvolatile variable resistor including a first electrode and a second electrode facing each other in a direction of a surface of a substrate and formed thereon, and a nonvolatile variable resistance body formed between the first electrode and the second electrode, comprises the steps of applying reduction scaling to a planar dimension of the first electrode; and applying magnification scaling to a height of the first electrode.

In a scaling method of a nonvolatile variable resistor according to an example embodiment~~the invention~~, the reduction scaling is applied at a magnification of 1/k times ($k > 1$), while the magnification scaling is applied at a magnification of k times.

~~In the invention, s~~Since a first electrode and a second electrode of a nonvolatile variable resistor formed on a substrate face each other in a direction of a surface of the substrate, an increase in resistance of the nonvolatile variable resistor can be suppressed in a case where scaling is applied to the nonvolatile variable resistor to reduce a projected area on a plane thereof. Especially, since a nonvolatile variable resistance body is formed on an outer surface of the first electrode and the second electrode is formed on an outer surface of the nonvolatile variable resistance body, layout thereof and the like are easy, which enables a nonvolatile variable resistor suitable for a memory device with a large capacity to be realized. Furthermore, since the nonvolatile variable resistance body is made of a manganese oxide of a perovskite structure, it is possible to obtain a nonvolatile

variable resistor having a stable change in resistance thereof suitable for a memory device.

~~In the invention, s~~Since a memory cell is constituted of a nonvolatile variable resistor formed on a substrate so that a first electrode and a second electrode face each other in a direction of a surface thereof, an increase in resistance of the nonvolatile variable resistor can be suppressed and no operation speed (an access time) of the memory device is reduced in a case where scaling is applied to the nonvolatile variable resistor to reduce a projected area on a plane thereof. Especially, in a case where scaling is applied to the nonvolatile variable resistor in a 1T1R type memory cell or a 1D1R type memory cell to reduce a projected area on a plane thereof, an increase in resistance of the nonvolatile variable resistor can be suppressed and no operation speed (an access time) of the memory device is reduced.

~~In the invention, s~~Since magnification scaling is applied to the direction of a height in a case where reduction scaling is applied to the nonvolatile variable resistor to reduce a projected area on a plane thereof, it is possible to use a scaling method of a nonvolatile variable resistor capable of suppressing an increase in resistance thereof.

The above and further objects and features ~~of the invention~~ will more fully be apparent from the following detailed description with accompanying drawings.

Please amend the paragraph beginning at page 19, line 7, and continuing to page 19, line 21, as follows:

Figs. 1A and 1B are descriptive views showing a way of scaling in ~~a~~ nonvolatile variable resistor according to a first embodiment. Fig. 1A is a perspective view of the nonvolatile variable resistor Rv before scaling is applied. Fig. 1B is a perspective view of the nonvolatile variable resistor Rv after scaling is applied at a magnification of 1/k times ($k > 1$) thereto. In Fig. 1A, the nonvolatile variable resistor Rv is formed with a first electrode 1 in the shape of a column of a height h and a radius r as an inner

electrode. A nonvolatile variable resistance body 2 in a cylindrical shape is formed on an outer surface of the first electrode 1 in a layer with a film thickness t and a second electrode 3 in a cylindrical shape of a radius r + t is formed as an outer electrode on an outer surface of the nonvolatile variable resistance body 2 so as to face the first electrode 1.

Please amend the paragraph beginning at page 20, line 13, and continuing to page 21, line 5, as follows:

In Fig. 1A, since a surface area So of the first electrode 1 facing the nonvolatile variable resistance body 2 is $2\pi rh$ and a film thickness is t, a resistance Ro before scaling is applied approximates $Ro = \rho t/2\pi rh$ using the surface area So of the first electrode 1. In Fig. 1B after scaling is applied, a surface area Ss of the first electrode 1 facing the nonvolatile variable resistance body 2 is $2\pi rh/k$. A resistance Rs after scaling is applied in a case where no scaling is applied to a film thickness t is $\rho t/Ss = \rho tk/2\pi rh = kRo$. Therefore, in a case where scaling is applied at a magnification of 1/k times, a ratio of the resistance Rs after scaling and the resistance Ro before scaling is k. This shows that scaling in a nonvolatile variable resistor Rv of the ~~invention~~ embodiment takes a resistance of a value as low as k times that before scaling as compared with an increased resistance of a value k^2 times that before scaling in scaling in a conventional nonvolatile variable resistor Rv, showing it possible to suppress an increase in resistance in the ~~invention~~embodiment.

Please amend the paragraph beginning at page 23, line 20, and continuing to page 24, line 8, as follows:

~~Note that in the invention, a~~A manganese oxide of a perovskite structure has been used as the nonvolatile variable resistance body 2. Especially, as manganese oxides, any of materials expressed by $Pr_{(1-x)}Ca_xMnO_3$~~Pr.sub.(1-x)Ca.sub.xMnO.sub.3~~, $La_{(1-x)}Ca_xMnO_3$~~La.sub.(1-x)Ca.sub.xMnO.sub.3~~ and $La_{(1-x-y)}Ca_xPb_yMnO_3$~~La.sub.(1-x-y)Ca.sub.xPb.sub.yMnO.sub.3~~ showed a stable and good storage characteristic (generation of a change in resistance accompanied by application of a pulse). To be more ~~concrete~~specific, $Pr_{0.7}Ca_{0.3}MnO_3$~~Pr.sub.0.7Ca.sub.0.3MnO.sub.3~~, $La_{0.65}Ca_{0.35}MnO_3$~~La.sub.0.65Ca.sub.0.35MnO.sub.3~~ and $La_{0.65}Ca_{0.175}Pb_{0.175}MnO_3$~~La.sub.0.65Ca.sub.0.175Pb.sub.0.175MnO.sub.3~~ each showed a good storage characteristic. A film of the nonvolatile variable resistance body 2 was formed by means of sputtering and patterning thereon was conducted with photolithography.

Please amend the paragraphs beginning at page 39, line 17, and continuing to page 40, line 17, as follows:

In the ~~invention~~technology described herein, a nonvolatile variable resistor in which an increase in resistance due to scaling is suppressed can be realized in a case where scaling is applied to reduce a projected area on a plane of the nonvolatile variable resistor.

In the technology described herein~~invention~~, there can be realized a memory device with a large capacity in which no reduction in an operating speed (an access time) occurs since an increase in resistance of a nonvolatile variable resistor due to scaling can be suppressed in a case where scaling is applied to a nonvolatile variable resistor constituting the memory cell to reduce a projected area on a plane of the memory cell.

In the technology described hereinin~~vention~~, there can be realized a scaling method of a nonvolatile variable resistor capable of suppressing an increase in resistance due to scaling by applying magnification scaling to the direction of a height in a case where an reduction scaling is applied to reduce a projected area on a plane of the nonvolatile variable resistor.

As this ~~invention~~ technology may be embodied in several forms without departing from the spirit of essential characteristics thereof, the present embodiments are therefore illustrative and not restrictive, since the scope of the invention is defined by the appended claims rather than by the description preceding them, and all changes that fall within metes and bounds of the claims, or equivalence of such metes and bounds thereof are therefore intended to be embraced by the claims.